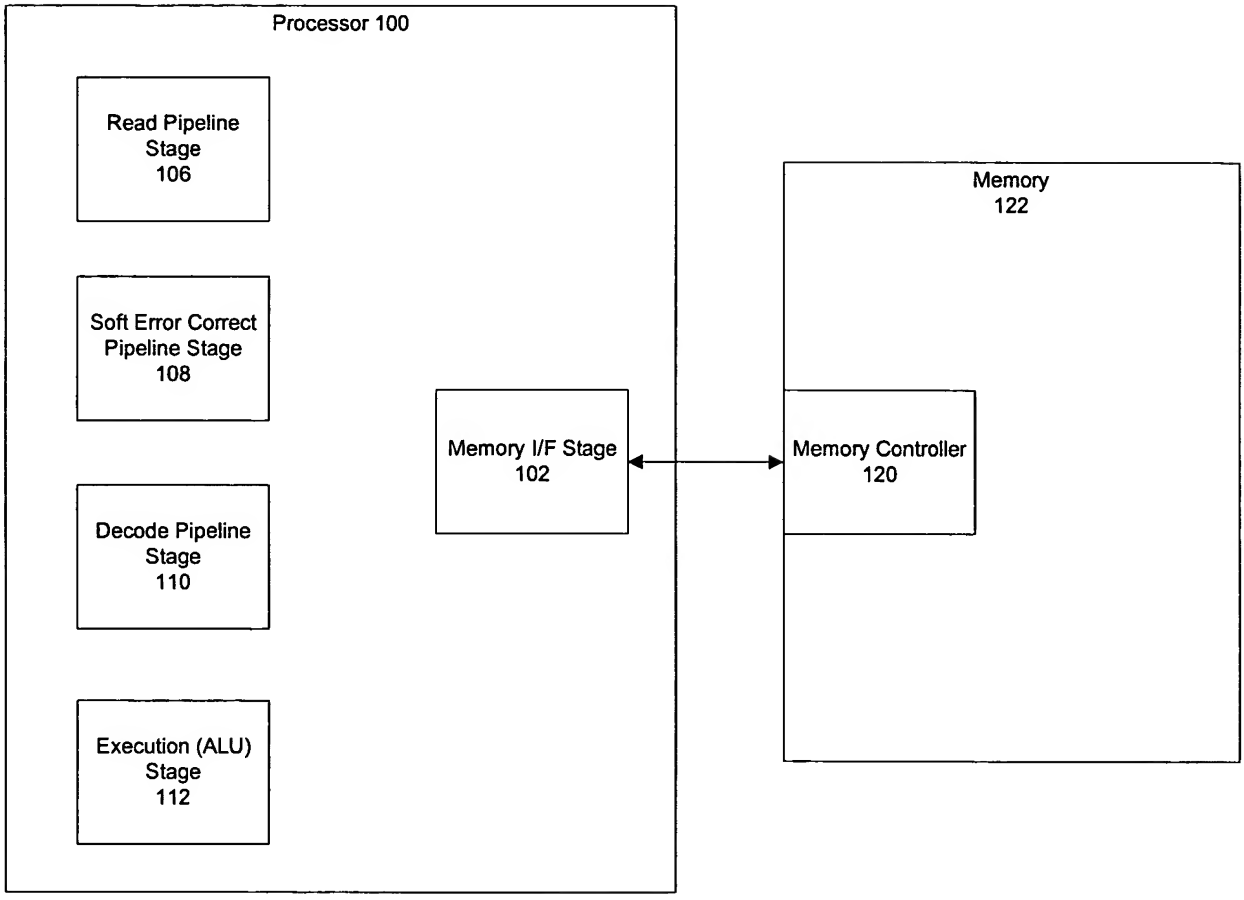
Figure 1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Read Pipeline Stage 106
Soft Error Correct Pipeline Stage 108
Decode Pipeline Stage 110
Execution (ALU) Stage 112
Memory I/F Stage 102
Memory 122
Memory Controller 120

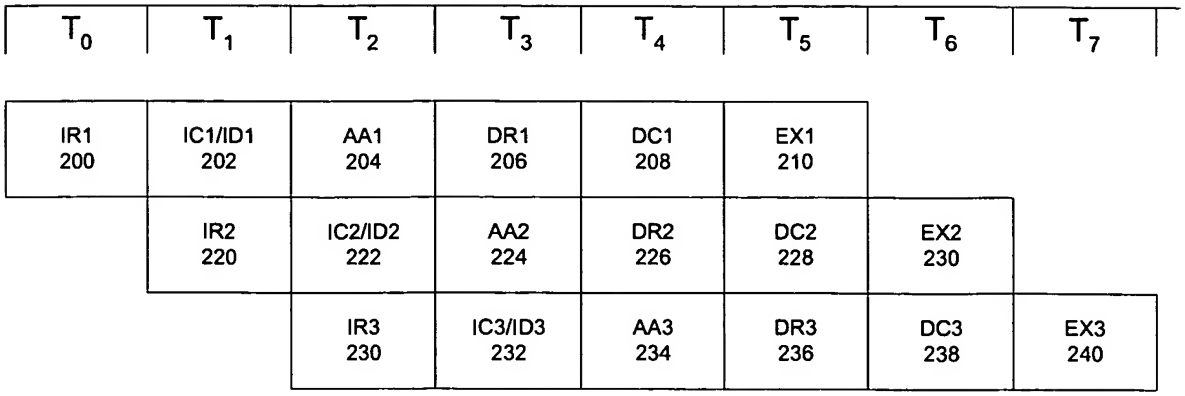


Figure 2

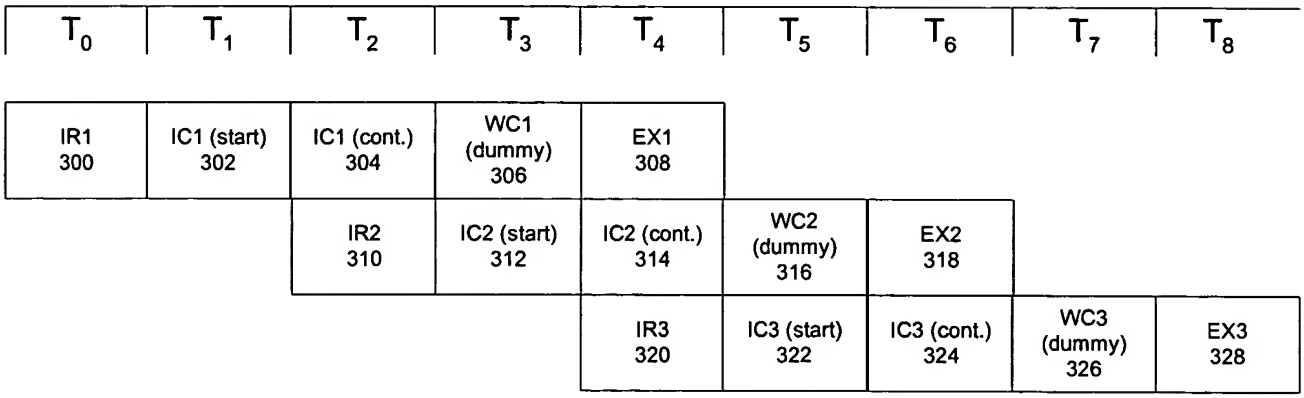
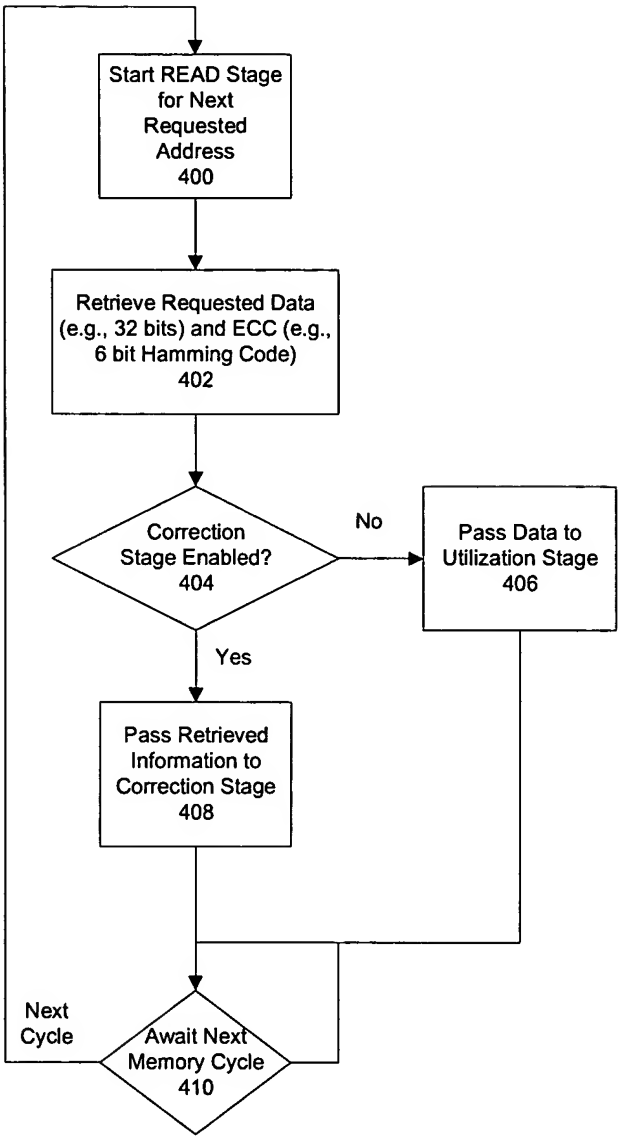


Figure 3



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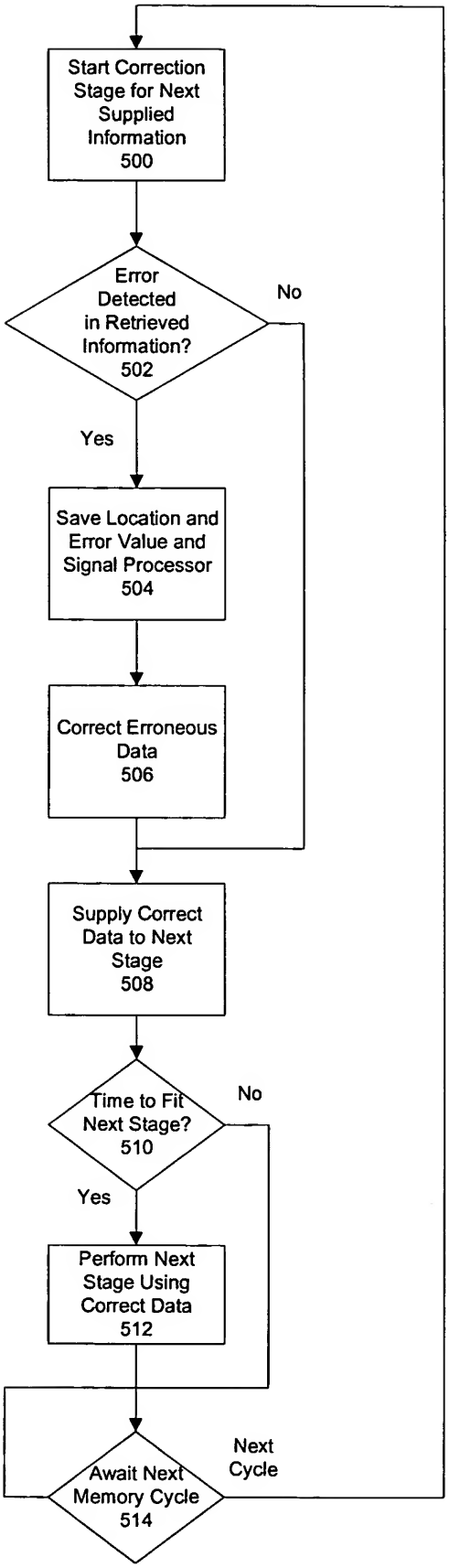

Figure 5

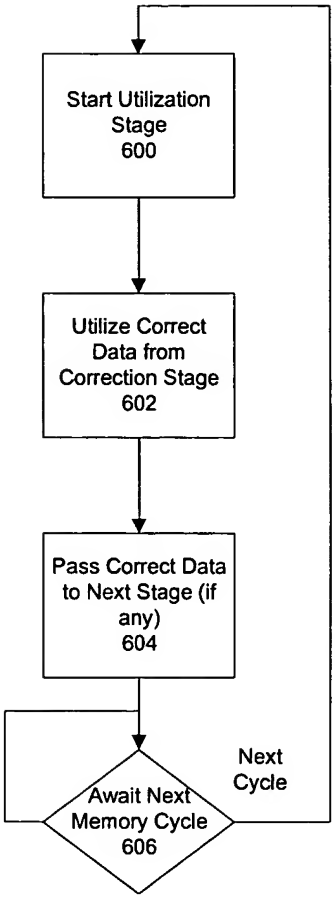

Figure 6

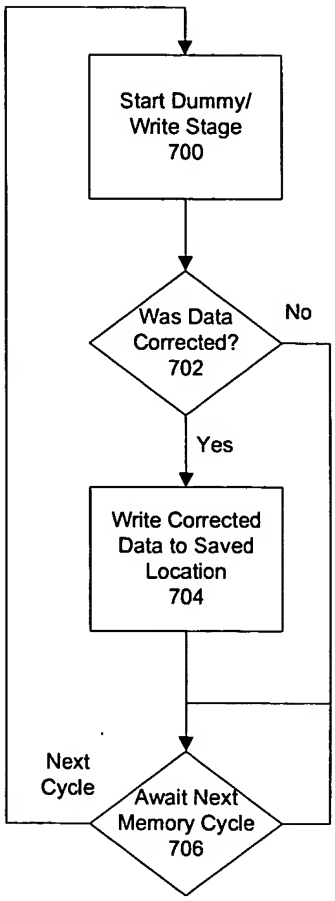

Figure 7